IN THE CLAIMS

This listing of the claim will replace all prior versions and listings of claim in the present application.

Listing of Claims

1. (currently Amended) An information processing device which processes information using a plurality of processors, comprising:

one or more first processors that have one or a plurality of first local memories;

one or more second processors which performs one of directly writing write ~~write~~ information into a target first local memory that a target first processor, selected from among said first processors, has, ~~and/or which~~and directly reading read ~~read~~ information from said target first local memory; ~~and~~

~~an~~ address map memory means for storing a first address map ~~on~~ in which the first local memory addresses for each of said one or more first processors are recorded,

wherein each of said one or more second processors performs one of acquiring ~~acquires~~ the first local memory address of said target first processor from said first address map, ~~writes~~ writing said write information into the acquired first local memory address, ~~and/or reads~~and reading said read information from the acquired first local memory address~~.~~; and

a relay device which receives said write information from said one or more second processors and transfers the write information to said target first processor,

wherein said relay device comprises:

a relay memory, and

wherein when transferring said write information, said relay device selectively performs an operation of said transfer after said write information is temporarily stored in said relay memory, or an operation of said transfer without storing said write information in said relay memory.

2. (Canceled).

3. (currently amended) The information processing device according to claim 1, further comprising:

one or a plurality of second local memories belonging to each of said one or more second processors;

a first address map memory means for storing a first address map on which the first local memory addresses for each of said one or more first processors are recorded; and

a second address map memory means for storing a second address map on which second local memory addresses for each of said one or more second processors are recorded;

wherein a target second microprocessor selected from among said one or more second processors acquires a first local memory write address indicating where writing is to be performed in said target first local memory from said first address map, and writes write information into said acquired first local memory address, and

wherein when said write information that has been written into said first local memory write address is a read command, said target first processor, in response to said read command, acquires the second local memory write

address indicating where writing is to be performed in said target second local memory on the target second processor that originated said read command from said second address map, reads out information in said first local memory, and writes said information into said acquired second local memory write address.

Claim 4 (canceled).

5. (Currently Amended) The information processing device according to claim 4, further comprising:

one or a plurality of first devices that have said one or more first processors,

wherein said relay device further comprises:

one or a plurality of transmitting parts which are respectively connected to the said one or a plurality of first devices, and which respectively transmit the received write information to said one or a plurality of first devices, and

wherein when write information received from a certain second device is to be transmitted to the target first device that has said target first processor, if the target transmitting part that is to transmit this write information is not in a busy state, the received write information is transmitted to the target first device from said target transmitting part without being stored in the relay memory, while if said target transmitting part is in a busy state, the write information is temporarily stored in the relay memory, and this write information is read out from the relay memory and transmitted to said target

first device from the target transmitting part when the busy state of said target transmitting part is released.

6. (Original) The information processing device according to claim 4, wherein one or more write information storage regions respectively corresponding to one or more transmission sources or transmission destinations of the write information are provided in said relay memory, and when temporarily storing the received write information in the relay memory, the relay device stores this write information in the target write information storage region corresponding to the transmission source or transmission destination, and in such cases, furthermore, if the amount of information accumulated in said target write information storage region exceeds a first threshold value, a notification of exceeding the first threshold value, which indicates that this threshold value has been exceeded, is transmitted to a specified second device, and the second device that receives said notification of exceeding the first threshold value reduces the frequency with which write information is issued or the amount of write information that is issued to said target local memory or said target first processor.

7. (currently amended) ~~The~~ An information processing device which processes information using a plurality of processors, comprising:

one or more first processors that have one or a plurality of first local memories;

one or more second processors which performs one of directly writing write information into a target first local memory that a target first processor,

selected from among said first processors, has, and directly reading read information from said target first local memory;

address map memory means for storing a first address map in which the first local memory addresses for each of said one or more first processors are recorded,

wherein each of said one or more second processors performs one of acquiring the first local memory address of said target first processor from said first address map, writing said write information into the acquired first local memory address, and reading said read information from the acquired first local memory address; ~~according to claim 4~~,

a relay device which receives said write information from said one or more second processors and transfers the write information to said target first processor,

wherein said relay device comprises:

a relay memory, and

wherein when transferring said write information, said relay device selectively performs an operation of said transfer after said write information is temporarily stored in said relay memory, or an operation of said transfer without storing said write information in said relay memory, and

wherein one or more write information storage regions respectively corresponding to said one or more transmission sources or transmission destinations are provided in said relay memory, and when temporarily storing the received write information in the relay memory, the relay device stores this write information in a target write information storage region corresponding to the transmission source or transmission destination, and in such cases,

furthermore, if the amount of information accumulated in the target write information storage region exceeds a second threshold value, notification of exceeding the second threshold value, which indicates that this threshold value has been exceeded, is transmitted to a specified second device, this second device selectively executes the operation of a direct write system in which said write information is directly written into the target local memory, or the operation of an indirect write system which is devised so that said write information is stored in the relay memory, and so that said target first processor can acquire this write information from the relay memory, and when said notification of exceeding the second threshold value is not received, the write information is transmitted by said direct write system, while when said notification of exceeding the second threshold value is received, the write information is transmitted by said indirect write system.

8. (currently amended) ~~The~~ An information processing device which processes information using a plurality of processors, comprising:

one or more first processors that have one or a plurality of first local memories;

one or more second processors which performs one of directly writing write information into a target first local memory that a target first processor, selected from among said first processors, has, and directly reading read information from said target first local memory;

address map memory means for storing a first address map in which the first local memory addresses for each of said one or more first processors are recorded,

wherein each of said one or more second processors performs one of acquiring the first local memory address of said target first processor from said first address map, writing said write information into the acquired first local memory address, and reading said read information from the acquired first local memory address;,

a relay device which receives said write information from said one or more second processors and transfers the write information to said target first processor,

wherein said relay device comprises:

a relay memory, and

wherein when transferring said write information, said relay device selectively performs an operation of said transfer after said write information is temporarily stored in said relay memory, or an operation of said transfer without storing said write information in said relay memory, ~~according to claim 6~~,

wherein one or more write information storage regions respectively corresponding to one or more transmission sources or transmission destinations of the write information are provided in said relay memory, and when temporarily storing the received write information in the relay memory, the relay device stores this write information in the target write information storage region corresponding to the transmission source or transmission destination, and in such cases, furthermore, if the amount of information accumulated in said target write information storage region exceeds a first threshold value, a notification of exceeding the first threshold value, which indicates that this threshold value has been exceeded, is transmitted to a

specified second device, and the second device that receives said notification of exceeding the first threshold value reduces the frequency with which write information is issued or the amount of write information that is issued to said target local memory or said target first processor, and

wherein if the amount of information accumulated in said target write information storage region exceeds the second threshold value that is larger than said first threshold value, the relay device transmits a notification of exceeding the second threshold value, which indicates that this threshold value has been exceeded, to said second device, said second device selectively executes the operation of a direct write system in which the write information is directly written into the target local memory, or the operation of an indirect write system which is devised so that the write information is stored in the relay memory, and so that said target first processor can acquire this write information from the relay memory, and when said notification of exceeding the second threshold value is not received, even though the notification of exceeding the first threshold value is received, the write information is transmitted by said direct write system, while when said notification of exceeding the second threshold value is received, said direct write system is stopped, and the write information is transmitted by said indirect write system.

9. (Original) The information processing device according to claim 7, wherein after the second device that has received said notification of exceeding the second threshold value has selected said indirect write system,

this second device stops the indirect write system and selects said direct write system in at least one of the following cases (1) and (2):

(1) a case in which the amount of information in said target information storage region is equal to or less than a third threshold value which is smaller than said second threshold value, and

(2) a case in which a fixed time has elapsed in the state in which said indirect write system was selected.

10. (Currently Amended) The information processing device according to claim 1, further comprising:

one or a plurality of first devices that have said one or more first processors;

one or a plurality of second devices that have said one or more second processors; and

a relay device that relays said write information from said second devices to said first device that has the target first processor;

wherein said relay device has one or a plurality of transmitting parts that respectively transmit information to said one or a plurality of first devices, and one or a plurality of receiving parts that respectively receive information from said one or a plurality of second devices, and each of said one or a plurality of transmitting parts and each of the said one or a plurality of receiving parts operate independently of each other.

11. (Original) The information processing device according to claim 1, wherein one or more local storage regions respectively corresponding to

said one or more second processors are provided in the local memories of each of said one or more first processors, each of said one or more second processors stores an address map on which the local memory address of said local storage region corresponding to this second processor is recorded for each first processor, and when the write information is written into the local memory of the target first processor, the local memory address corresponding to this target first processor is acquired from said address map, and the write information is written into this acquired local memory address.

12. (previously presented) The information processing device according to claim 1, further comprising a relay device which receives said write information including the local memory address of the target first processor from said one or more second processors, and transfers this write information to said target first processor, wherein each of said one or more second processors is connected via the relay device so as to be able to respectively communicate with said one or more first processors by one or more logical or physical paths, the relay device stores one or more local memory addresses respectively corresponding to said one or more paths for each second processor, and when transferring said received write information, a target path corresponding to said local memory address contained in said received write information is specified, and the write information is transferred to said target first processor via the specified target path.

13. (currently amended) A memory control device which comprises a plurality of microprocessors and a physical or logical memory device, and which performs memory control of the storage of information from host devices in said memory device using said plurality of microprocessors, comprising:

one or more first microprocessors that have one or a plurality of first local memories;

one or more second microprocessors; and

a first address map memory part that stores a first address map on which the first local memory addresses for each of said one or more first microprocessors are recorded;

wherein each of said one or more second microprocessors acquires, from said first address map, a first local memory write address indicating where writing is to be performed in a target first local memory, which a target first microprocessor selected from among said first microprocessors, has, and writes write information into the acquired first local memory write address;

a relay device which receives said write information from said one or more second processors and transfers the write information to said target first processor,

wherein said relay device comprises:

a relay memory, and

wherein when transferring said write information, the relay device selectively performs an operation of this transfer after the write information has been temporarily stored in the relay memory, or an operation of this transfer without storing the write information in the relay memory

14. (previously presented) The memory control device according to claim 13, further comprising:

one or a plurality of first devices in which said one or more first microprocessors are mounted;

one or a plurality of second devices in which said one or more second microprocessors are mounted; and

a relay device which relays communications between said one or a plurality of first devices and said one or a plurality of second devices;

wherein one or more local storage regions that respectively correspond to said one or more second microprocessors are provided in said first local memories,

first local memory addresses of the one or more local storage regions that respectively correspond to said one or more first microprocessors are recorded on said first address map, each of said one or more second microprocessors can be connected via the relay device so as to be able to respectively communicate with said one or more first microprocessors by one or more logical or physical paths, and furthermore, when outputting said write information, the second microprocessors acquire the first local memory address of the first local storage region corresponding to said target first processor from said first address map, and output write information which has first transmission destination information that includes said acquired first local memory address, the relay device stores one or more sets of second transmission destination information that respectively correspond to said one or more paths, and when transferring the received write information, the relay

device specifies the target path based on said first and second transmission destination information, and transmits the write information to said target first device via the specified target path, and the target first device writes the write information received from the relay device into the first local memory address that is included in the write information.

15. (currently amended)The memory control device ~~according to claim 14~~ which comprises a plurality of microprocessors and a physical or logical memory device, and which performs memory control of the storage of information from host devices in said memory device using said plurality of microprocessors, comprising:

one or more first microprocessors that have one or a plurality of first local memories;

one or more second microprocessors;

a first address map memory part that stores a first address map on which the first local memory addresses for each of said one or more first microprocessors are recorded,

wherein each of said one or more second microprocessors acquires, from said first address map, a first local memory write address indicating where writing is to be performed in a target first local memory, which a target first microprocessor selected from among said first microprocessors, has, and writes write information into the acquired first local memory write address~~.~~;

one or a plurality of first devices in which said one or more first microprocessors are mounted;

one or a plurality of second devices in which said one or more second microprocessors are mounted; and

a relay device which relays communications between said one or a plurality of first devices and said one or a plurality of second devices;

wherein one or more local storage regions that respectively correspond to said one or more second microprocessors are provided in said first local memories,

first local memory addresses of the one or more local storage regions that respectively correspond to said one or more first microprocessors are recorded on said first address map, each of said one or more second microprocessors can be connected via the relay device so as to be able to respectively communicate with said one or more first microprocessors by one or more logical or physical paths, and furthermore, when outputting said write information, the second microprocessors acquire the first local memory address of the first local storage region corresponding to said target first processor from said first address map, and output write information which has first transmission destination information that includes said acquired first local memory address, the relay device stores one or more sets of second transmission destination information that respectively correspond to said one or more paths, and when transferring the received write information, the relay device specifies the target path based on said first and second transmission destination information, and transmits the write information to said target first device via the specified target path, and the target first device writes the write information received from the relay device into the first local memory address that is included in the write information

wherein said relay device comprises:

a relay memory, and

wherein when transferring said write information, the relay device selectively performs an operation of this transfer after the write information has been temporarily stored in the relay memory, ~~and~~or an operation of this transfer without storing the write information in the relay memory.

16. (Original) The memory control device according to claim 14, wherein said relay device is communicably connected to said one or a plurality of first devices, further comprises one or a plurality of transmitting parts that respectively transmit the received write information to said one or a plurality of first devices, and when transferring write information received from a certain second device to said target first device, if the target path is not in a busy state, the received write information is transmitted to the target first device via the this target path without being stored in the relay memory, while if the target path is in a busy state, the write information is temporarily stored in the relay memory, and when the busy state of the target path is released, the write information is read out from the relay memory and transmitted to the target first device via the target path.

17. (Original) The memory control device according to claim 15, wherein one or more write information storage regions respectively corresponding to one or more transmission sources or transmission destinations of the write information are provided in said relay memory, and when the received write information is temporarily stored in the relay memory,

said relay device stores this write information in a target write information storage region corresponding to the transmission source or transmission destination, and in such cases, furthermore, if the amount of information accumulated in the target write information storage region exceeds the first threshold value, a notification of exceeding the first threshold value, which indicates that this threshold value has been exceeded, is transmitted to a specified second device, and the second device that has received this notification of exceeding the first threshold value has been exceeded reduces the frequency with which write information is issued or the amount of write information that is issued to said target local memory or said target first microprocessor.

18. (Original) The memory control device according to claim 14, wherein said relay device comprises one or a plurality of transmitting parts that respectively transmit information to said one or a plurality of first devices, and one or a plurality of receiving parts that respectively receive information from said one or a plurality of second devices, each of said one or a plurality of transmitting parts and each of said one or a plurality of receiving parts operate independently from each other.

19. (Original) The memory control device according to claim 18, wherein said relay device comprises a receiving buffer that is separate from said relay memory, each of said one or a plurality of receiving parts once store the write information received from said second devices in this receiving buffer.

20. (currently amended) A memory control device which comprises a plurality of microprocessors and a physical or logical memory device, and which controls the storage of information from host devices in said memory device using said plurality of microprocessors, this memory control device comprising:

one or more first microprocessors that have one or a plurality of first local memories;

one or more second microprocessors that have one or a plurality of second local memories;

a first address map memory means for storing a first address map on which first local memory addresses for each of said one or more first microprocessors are recorded; and

a second address map memory means for storing a second address map on which second local memory addresses for each of said one or more second microprocessors are recorded;

wherein a target second microprocessor selected from among said second microprocessors acquires, from the first address map, a first local memory write address indicating where writing is to be performed in a target first local memory which a target first microprocessor selected from among said first microprocessors has, and writes a read command into the acquired first local memory write address, and;

wherein in response to the read command that is written into the first local memory write address, the target first microprocessor acquires, from the second address map, the second local memory write address of the target second microprocessor that originated said read command, reads out read

information in the first local memory, and writes the read information into the acquired second local memory write address~~.~~,

a relay device which receives said write information from said one or more second processors and transfers the write information to said target first processor,

wherein said relay device comprises:

a relay memory, and

wherein when transferring said write information, the relay device selectively performs an operation of this transfer after the write information has been temporarily stored in the relay memory, or an operation of this transfer without storing the write information in the relay memory.

21. (currently amended) An information processing method which processes information using a plurality of processors, comprising the steps in which:

each of one or more second microprocessors acquires a local memory address of a target first processor from an address map ~~on~~ in which local memory addresses for each of one or more first processors having one or a plurality of local memories are recorded; ~~and~~

each of said one or more second processors ~~writes~~ performs one of writing write information into said acquired local memory address, ~~and/or reads~~ and reading read information from said acquired local memory address~~.~~, and

a relay device which receives said write information from said one or more second processors and transfers the write information to said target first processor,

wherein said relay device comprises:

a relay memory, and

wherein when transferring said write information, said relay device selectively performs an operation of said transfer after said write information is temporarily stored in said relay memory, or an operation of said transfer without storing said write information in said relay memory.

22. (currently amended) An information processing device which processes information using a plurality of processors, comprising:

one or more first processors that have one or a plurality of first local memories;

one or more second processors which performs one of directly ~~write~~ writing write information into a target first local memory that a target first processor selected from among said first processors has, ~~and/or which~~and directly ~~read~~ reading read information from said target first local memory; and

a relay device which receives said write information from said one or more second processors and transfers the write information to said target first processor,

wherein said relay device comprises a relay memory, and

wherein when transferring said write information, said relay device selectively performs an operation of said transfer after said write information is

temporarily stored in said relay memory, or an operation of said transfer without storing said write information in said relay memory.

23. (previously presented) An information processing method which processes information using a plurality of processors, comprising the steps in which:

each of one or more second microprocessors acquires a local memory address of a target first processor from an address map on which local memory addresses for each of one or more first processors having one or a plurality of local memories are recorded; and

each of said one or more second processors writes write information into said acquired local memory address, and/or reads read information from said acquired local memory address; and

a relay device receives said write information from said one or more second processors and transfers the write information to said target first processor, wherein said relay device comprises a relay memory, and when transferring said write information, said relay device selectively performs an operation of said transfer after said write information is temporarily stored in said relay memory, or an operation of said transfer without storing said write information in said relay memory.

24. (new) An information processing device according to claim 1, wherein said relay device comprises:

a buffer that is separate from said relay memory, when transferring said write information, the relay device selectively performs an operation of

said transfer after said write information is stored in said relay memory, an operation of said transfer after said write information is temporarily stored in said buffer.

25. (new) A memory control device according to claim 13, wherein said relay device comprises:

a buffer that is separate from said relay memory, when transferring said write information, the relay device selectively performs an operation of said transfer after said write information is stored in said relay memory, an operation of said transfer after said write information is temporarily stored in said buffer.

26. (new) A memory control device according to claim 20, wherein said relay device comprises:

a buffer that is separate from said relay memory, when transferring said write information, the relay device selectively performs an operation of said transfer after said write information is stored in said relay memory, an operation of said transfer after said write information is temporarily stored in said buffer.

27. (new) An information processing method according to claim 21, wherein said relay device comprises:

a buffer that is separate from said relay memory, when transferring said write information, the relay device selectively performs an operation of said transfer after said write information is stored in said relay memory, an

operation of said transfer after said write information is temporarily stored in said buffer.

28. (new) An information processing method according to claim 22, wherein said relay device comprises:

a buffer that is separate from said relay memory, when transferring said write information, the relay device selectively performs an operation of said transfer after said write information is stored in said relay memory, an operation of said transfer after said write information is temporarily stored in said buffer.

29. (new) An information processing method according to claim 23, wherein said relay device comprises:

a buffer that is separate from said relay memory, when transferring said write information, the relay device selectively performs an operation of said transfer after said write information is stored in said relay memory, an operation of said transfer after said write information is temporarily stored in said buffer.

30. (new) An information processing device according to claim 24, wherein said relay further comprises:

a plurality of ports, when write information received via a certain port of the ports is to be transmitted to the target first processor, if other port is not in a busy state, the received write information is temporarily stored in the buffer, and this write information is transmitted from the buffer to the target first

processor via said other port, while if said other port is in a busy state, the write information is stored in the relay memory, and this write information is read out from the relay memory and transmitted to said target first processor via the other port when the busy state of said other port is released.

31. (new) A memory control device according to claim 25, wherein said relay further comprises:

a plurality of ports, when write information received via a certain port of the ports is to be transmitted to the target first processor, if other port is not in a busy state, the received write information is temporarily stored in the buffer, and this write information is transmitted from the buffer to the target first processor via said other port, while if said other port is in a busy state, the write information is stored in the relay memory, and this write information is read out from the relay memory and transmitted to said target first processor via the other port when the busy state of said other port is released.

32. (new) A memory control device according to claim 26, wherein said relay further comprises:

a plurality of ports, when write information received via a certain port of the ports is to be transmitted to the target first processor, if other port is not in a busy state, the received write information is temporarily stored in the buffer, and this write information is transmitted from the buffer to the target first processor via said other port, while if said other port is in a busy state, the write information is stored in the relay memory, and this write information is

read out from the relay memory and transmitted to said target first processor via the other port when the busy state of said other port is released.

33. (new) An information processing method according to claim 27, wherein said relay further comprises:

a plurality of ports, when write information received via a certain port of the ports is to be transmitted to the target first processor, if other port is not in a busy state, the received write information is temporarily stored in the buffer, and this write information is transmitted from the buffer to the target first processor via said other port, while if said other port is in a busy state, the write information is stored in the relay memory, and this write information is read out from the relay memory and transmitted to said target first processor via the other port when the busy state of said other port is released.

34. (new) An information processing method according to claim 28, wherein said relay further comprises:

a plurality of ports, when write information received via a certain port of the ports is to be transmitted to the target first processor, if other port is not in a busy state, the received write information is temporarily stored in the buffer, and this write information is transmitted from the buffer to the target first processor via said other port, while if said other port is in a busy state, the write information is stored in the relay memory, and this write information is read out from the relay memory and transmitted to said target first processor via the other port when the busy state of said other port is released.

35. (new) An information processing method according to claim 29, wherein said relay further comprises:

a plurality of ports, when write information received via a certain port of the ports is to be transmitted to the target first processor, if other port is not in a busy state, the received write information is temporarily stored in the buffer, and this write information is transmitted from the buffer to the target first processor via said other port, while if said other port is in a busy state, the write information is stored in the relay memory, and this write information is read out from the relay memory and transmitted to said target first processor via the other port when the busy state of said other port is released.

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